What is claimed is:

1. A semiconductor device, comprising:

a semiconductor device body exposing at least one silicon-containing portion;

a metal silicide layer with a first resistivity overlying the silicon-containing portion; and

a conductor layer with a second resistivity overlying the metal silicide layer, wherein the second resistivity is small than the first resistivity.

2. The semiconductor device as claimed in claim 1, wherein the conductor layer comprises the same type metal ion as that of the metal silicide layer.

3. The semiconductor device as claimed in claim 1, wherein the conductor layer comprises refractory metal.

4. The semiconductor device as claimed in claim 1, wherein the metal silicide layer comprises a silicide of refractory metal.

5. The semiconductor device as claimed in claim 1, wherein the conductor layer comprises a metal selected from a group consisting of Au, Pt, Ni, Co, Pd, W and Ti.

6. A resistance-reduced transistor, comprising:

a silicon substrate having a gate stack formed thereon, wherein the gate stack exposes a silicon gate electrode;

a pair of source/drain regions, oppositely disposed in the silicon substrate adjacent the gate stack; and

a metallized bilayer overlying each source/drain reigon and the silicon gate electrode to thereby respectively reduce resistance thereof, wherein the metallized bilayer comprises a metal top layer.

7. The transistor as claimed in claim 6, further comprising a metal silicide layer disposed between the metal top layer and each source/drain region and the silicon gate electrode.

8. The transistor as claimed in claim 6, wherein the metal top layer comprises the same type of metal ion as that of the metal silicide layer.

9. The transistor as claimed in claim 6, wherein the metal top layer comprises refractory metal.

10. The transistor as claimed in claim 6, wherein the metal silicide layer comprises a silicide of refractory metal.

11. The transistor as claimed in claim 6, wherein the metal top layer comprises metal selected from a group consisting of Au, Pt, Ni, Co, Pd, W and Ti.

12. A method of fabricating a semiconductor device, comprising the steps of:

providing a semiconductor device body exposing at least one silicon-containing portion;

selectively forming a metal silicide layer with a first resistivity over the silicon-containing portion; and

forming a conductor layer with a second resistivity on the metal silicide layer, wherein the second resistivity is smaller than the first resistivity.

13. The method as claimed in claim 12, wherein the conductor layer comprises the same type of metal ion as that of the metal silicide layer.

14. The method as claimed in claim 12, wherein the metal layer comprises refractory metal.

15. The method as claimed in claim 12, wherein the conductor silicide layer comprises a silicide of refractory metal.

16. The method as claimed in claim 12, wherein the metal layer comprises a metal selected from a group consisting of Au, Pt, Ni, Co, Pd, W and Ti.

17. The method as claimed in claim 12, wherein the conductor layer is formed by electroless plating.

18. The method as claimed in claim 17, wherein the electroless plating is performed in an electrolyte comprising at least a reducing agent, a catalyst, a complex agent and metal ions of the metal layer.

19. The method as claimed in claim 18, wherein the catalyst comprises Pd or metal ions of the conductor layer.

20. The method as claimed in claim 12, wherein a thickness ratio between the metal silicide layer and the conductor layer is about 1:1 to 1:10.

21. A method of fabricating a resistance-reduced transistor, comprising the steps of:

providing a silicon substrate having a gate stack formed thereon and a source/drain pair oppositely formed in each side of the substrate adjacent to the gate stack, wherein the gate stack comprises an exposed silicon gate electrode;

selectively forming a metal silicide layer over the source/drain regions and the exposed silicon gate electrode; and

selectively forming a metal layer over each metal silicide layer by electroless plating to respectively reduce resistance of each source/drain region and the exposed silicon gate electrode.

22. The method as claimed in claim 21, wherein the metal layer comprises the same type of metal ion as that of the metal silicide layer.

23. The method as claimed in claim 21, wherein the metal layer comprises refractory metal.

24. The method as claimed in claim 21, wherein the metal silicide layer comprises a silicide of refractory metal.

25. The method as claimed in claim 21, wherein the metal layer comprises a metal selected from a group consisting of Au, Pt, Ni, Co, Pd, W and Ti.

26. The method as claimed in claim 21, wherein the electroless plating is performed in an electrolyte comprising at least a reducing agent, a catalyst, a complex agent and metal ions of the metal layer.

27. The method as claimed in claim 26, wherein the catalyst comprises Pd or the metal ions of the metal layer.

28. The method as claimed in claim 21, wherein a thickness ratio between the metal silicide layer and the metal layer is about 1:1 to 1:10.